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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,432	11/25/2003	Astrid Elbe	20046/0200502-US0	6238

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EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/723,432	ELBE ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/25/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications on 4/19/2006 and replaces the action mailed on 3/14/2006.

2. Claims 1-13 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 11/25/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

Figure 6 and 7 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated.

See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 12 is objected because of the following informalities:

Claim 12 recites "each peripheral unit" in line 1. However, the parent claim 1 recites only one peripheral unit. For the rest of the office action, it is assumed that claim 12 depends on claim 11, since claim 11 recites the plurality of peripheral units.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801).

For claim 1, Williams et al teach the following limitations:

An electronic circuit (Fig 1) comprising:

a peripheral unit (15) having a clock connection (CHIP CLOCK) and a data connection ("DATA"), said clock connection being connected to an external clock input (CHIP CLOCK is external), so that the peripheral unit receives a second clock which is relatively prime with respect to the first clock and whose clock frequency has no

common divisor with the first clock (lines 58-59 of column 2 mention that the ratio can be 2:1, 3:2, 4:3. Thus, when the clock frequencies are chosen as 3 MHz and 4 MHz, there is no common divisor. The frequencies would be prime with respect to each other);

synchronization means (14 and 16) comprising a first and a second data connection (DATA is shown as two way connection in Fig 1 for receiving and transmitting data on the bus. Thus, it has at least two connection with bus), said first data connection being connected to said data connection of said peripheral unit (Fig 1);

and a data bus (11) being connected to said data connection of said central processing unit (BUS has to connect with processor to transfer BUS data to processor) and to said second data connection of said synchronization means (bus is connected to 14 and 16).

Williams et al do not explicitly mention the following limitations:

a central processing unit having a clock connection for receiving a first clock and a data connection. Fig 1 of Williams et al does not show the CPU though it shows the BUS and data transfer between BUS and peripheral chip.

The BUS must be connected to a processor for processing the transferred data from chip to BUS. Thus there must be a CPU that is able to process the data in BUS. It is not

mentioned that BUS clock is connected to the processor clock. However, BUS clock is often connected to processor clock in the simplified data processing system.

For claim 4, the circuit of Fig 1 is an integrated circuit.

For claim 13, Williams et al teach a method of controlling an electronic circuit (abstract) having a central processing unit (BUS 11 must be connected to a CPU, since the system is a data communication system) and a peripheral unit (15) being connected to each other via a data bus (11), comprising:

clocking said central processing unit by a first clock ("BUS CLOCK");

clocking said peripheral unit by a second clock which is different from the first clock ("CHIP CLOCK"), so that the clock frequency of the second clock is relatively prime with respect to the clock frequency of the first clock (lines 58-59 of column 2 mention that the ratio can be 2:1, 3:2, 4:3. Thus, when the clock frequency are chosen as 3 MHz and 4 MHz, there is no common divisor. The frequencies would be prime with respect to each other);

and synchronizing data transmitted between said central processing unit and said peripheral unit via said data bus (Fig 1 shows the synchronizing circuitry 16).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801), in view of Heinrich et al (US Patent 6470393), further in view of Yamaguchi (EP 0569131).

For claim 3, Williams et al do not teach any common chip card and controllable oscillator.

Heinrich et al teach a controllable oscillator (line 24 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Williams et al, since it provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

However, Williams et al as modified by Heinrich et al do not teach that the components are in a common chip card.

Yamaguchi teaches that the components of an integrated circuits are in a common chip card (Fig 1).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have the components in a common chip card, since that is typically done to create a microprocessor based system design. Providing all the components together in a common chip card increases portability and maintenance of a system, since the chip card can be replaced easily in case of failure.

5. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801), in view of Heinrich et al (US Patent 6470393).

For claim 5, William et al do not teach any controllable oscillator.

Heinrich et al teach a system where an electronic circuit comprises a controlling means having a control output that is connected to control input of a controllable oscillator and the control means control the oscillator depending on a control parameter (lines 2-5 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Williams et al, since it provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

For claim 6, control parameter depends on activity on the bus. Thus, the control parameter depends on the task performed by the peripheral unit (lines 3-5 of column 4 of Heinrich et al).

For claims 7 and 8, the chip clock of Williams et al do not have common divisor with bus clock and chip clock can be faster than bus clock. However, the clock does not come from a controllable oscillator.

Heinrich et al teach a controllable oscillator (line 24 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Williams et al, since controllable oscillator provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

6. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801), in view of applicant's admission of prior art.

For claim 9, applicant admits that conventional circuitry of Fig 6 is a cryptography controller.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Williams et al and Applicant's Admission of Prior Art. One ordinary skill in the art would have been motivated to have the cryptography controller, since cryptography is very useful tool for ensuring security.

For claim 10, AAPA shows 920a and 920b as coprocessors. Since, Fig 6 is a cryptography controller, it must process some cryptographic algorithm.

For claim 11, Fig 6 of AAPA comprises two coprocessors. However, AAPA does not mention that the peripheral unit being connected to oscillator.

Examiner takes an official notice that coprocessor connected to controllable oscillator is well known in the art.

One ordinary skill in the art would have been motivated to connect controllable oscillator to coprocessor, since controllable oscillator produce clock to operate the coprocessors.

For claim 12, the two coprocessors operate in parallel performing various tasks as mentioned in [0012] of AAPA. Since Fig 6 shows the cryptography controller, the tasks should be encrypting/decrypting.

Allowable Subject Matter

Claim 2 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100